UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/718,031	11/19/2003	Mark L. DiOrio	MTB005US1P	7148

27906 7590 02/24/2006

PATENT LAW OFFICES OF DAVID MILLERS
6560 ASHFIELD COURT
SAN JOSE, CA 95120

EXAMINER	
NGUYEN, JIMMY	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 02/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/718,031	DIORIO, MARK L.	
	Examiner	Art Unit	
	Jimmy Nguyen	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10; 13, 15 - 33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10; 13; 15 - 33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Response to Argument

The applicant's amendment filed 12/7/2005 has been considered with the following effect;

a. Applicant's arguments with respect to the rejection(s) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 7 – 9, 13, 15 – 18, 22 – 33 are rejected under 35 U.S.C. 102(b) as being anticipated by Hirano et al (US 5,625,298).

As to claim 1, Hirano et al disclose (fig 2) a probing system for testing a device comprising:

a probe comprising a semiconductor die (120) and probe tips (101) on the semiconductor die (120) wherein the probe tips (101) comprise bumps that are arranged in a pattern that matches a pattern of terminals (210) on the device (200) and that directly contact the terminals (210) during testing of the device; the probe tips (101) being affixed to the semiconductor dies (120) so that the pattern of the probe tips (101)

expands/contracts with thermal expansion/contraction of the semiconductor die (200); and

a tester (not shown, column 3 line 44) electrically connected to the probe tips (101).

As to claims 2, 32, Hirano et al disclose (fig 2) the system of claim 1, wherein the device (200) comprises a semiconductor material (silicon) that is substantially the same as material in the semiconductor die (120).

As to claims 7, 17, Hirano et al disclose (fig 1) the system of claim 1, wherein the semiconductor die comprises:

terminals (not label, but connected to the traces) on a bottom surface of the semiconductor die (120); and

conductive vias (not label, see fig 1) that pass through the semiconductor die (120) and provide electrical connections between the probe tips (101) on a top surface of the die (120) and the terminals on the bottom surface.

As to claims 8, 30, Hirano et al disclose (fig 2) the system of claim 7, wherein the probe further comprises a substrate (200) on which the semiconductor die is mounted, wherein the terminals (101) of the semiconductor die (120) directly contact the substrate (200).

As to claim 9, Hirano et al disclose (fig 2) the system of claim 8, further comprising a probe card, wherein terminals (210) on the substrate (200) directly contact the probe card.

As to claim 13, Hirano et al disclose (fig 2) a method for forming a probe for electrical testing of a semiconductor device comprising;

Form a probe comprising a semiconductor die (120) on which probe tips (101) are arranged in a pattern that matches a pattern of terminals (210) on the device (200); therefore Hirano et al teach the method of forming probe tips wherein forming the probe tips comprises:

Form contact pads on the semiconductor die (120); therefore Hirano et al teach the method of forming contact pad; and

Form conductive bumps (101) on a surface of the contacts pads (the interconnection); therefore Hirano et al teach the method of forming conductive bump; and

Fabricate an interconnect structure (130) for electrical connection of the probe tips (101) to test equipment (not shown); therefore Hirano et al teach the method of fabricating.

As to claims 15, 22, 29, Hirano et al disclose (fig 2) the method of claim 13 wherein fabricating the interconnect structure comprises forming conductive traces

(130) or contact pads on a surface of the semiconductor die (120) on which the probe tips (101) reside.

As to claim 16, Hirano et al disclose (fig 2) the method of claim 15, further comprising wire bonding the conductive traces to a substrate.

As to claim 18, Hirano et al disclose (fig 2) the method of claim 17, wherein forming the conductive vias comprises:

Form holes in semiconductor die (vias); therefore Hirano et al teach the method of forming hole and

Fill the holes with a conductive material; therefore Hirano et al teach the method of filling hole.

As to claim 23, Hirano et al disclose (fig 2) the method further comprising attaching the terminals (101) to an interconnect substrate 130.

As to claim 24, Hirano et al disclose (fig 2) the method further attaching terminal comprises performing a solder reflow process (for attaching the solder bumps 101).

As to claims 25, **26**, Hirano et al disclose (fig 2) the method of forming probe tips (101) further comprises planarizing the bumps (101) and planarizing comprises chemical mechanical polishing.

As to claims 27, **28**, Hirano et al disclose (fig 2) the method of forming contact pads (101) on the semiconductor die (120) comprises a manufacturing process or mask that is substantially identical to a process used in fabricating contact pads (210) on the semiconductor device to be tested (200).

As to claim 31, Hirano et al disclose (fig 2) the system wherein surfaces of the bumps (101) that contact the device are planar (when it comes to contact with dut) and in the same plane.

As to claim 33, Hirano et al disclose (fig 2) the bumps (101) are of a type suitable for use in a flip chip package.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3 – 6 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirano et al (US 5,625,298) in view of Nakajima et al (US 5804983).

As to claim 3, Hirano et al disclose (fig 2) a probing system for testing a device comprising:

a probe comprising a semiconductor die (120) and probe tips (101) on the semiconductor die (120) wherein the probe tips (101) comprise bumps that are arranged in a pattern that matches a pattern of terminals (210) on the device (200) and that directly contact the terminals (210) during testing of the device; the probe tips (101) being affixed to the semiconductor dies (120) so that the pattern of the probe tips (101) expands/contracts with thermal expansion/contraction of the semiconductor die (200); and

a tester (not shown, column 3 line 44) electrically connected to the probe tips (101).

However, Hirano et al are silent on a probe card including a receptacle in which the probe is detachably mounted, wherein the tester makes electrical connections to the probe tips through the probe card.

On the other hand, Nakajima et al disclose (fig 1) the system of claim 1 further comprising a probe card (22) including a receptacle (25, card holder) in which the probe (22) is detachably mounted (column 5 lines 65 – 67) , wherein the tester (28) makes electrical connections to the probe tips (23) through the probe card (22).

It would have been obvious to one having an ordinary skill in the art at the time of the invention was made to modify the probe card of Hirano et al with the receptacle probe card of Nakajima et al for the purpose of replacing different probe card to match with different device under test.

As to claim 4, The combination of Hirano et al and Nakajima et al disclose the system of claim 3, wherein the probe further comprises a substrate (120) on which the semiconductor die is mounted; further, Nakajima et al disclose the receptacle (25) being sized to hold the substrate (22).

As to claim 5, Hirano et al disclose (fig 2) the system of claim 1, wherein the device (120) comprises a semiconductor material (silicion) that is substantially the same as material in the semiconductor die.

As to claim 6, Hirano et al disclose (fig 2) the system of claim 4 and the method of claim 13, wherein the semiconductor die (120) comprises contact pads (101) to which respective probe tips are attached, and wire bonds (130) electrically connect the contact pads (101) to the substrate (120).

As to claim 10, Hirano et al disclose (fig 2) a probing system for testing a device comprising:

a probe comprising a semiconductor die (120) and probe tips (101) on the semiconductor die (120) wherein the probe tips (101) comprise bumps that are arranged in a pattern that matches a pattern of terminals (210) on the device (200) and that directly contact the terminals (210) during testing of the device; the probe tips (101) being affixed to the semiconductor dies (120) so that the pattern of the probe tips (101) expands/contracts with thermal expansion/contraction of the semiconductor die (200); and

a tester (not shown, column 3 line 44) electrically connected to the probe tips (101).

However, Hirano et al are silent on a positioning system adapted to position the probe relative to the device so that the probe tips contact the terminals on the device.

On the other hand, Nakajima et al disclose (fig 1) the system of claim 1 further comprising a positioning system (17) adapted to position the probe (23) relative to the device (14) so that the probe tips (23) contact the terminals on the device (14).

It would have been obvious to one having an ordinary skill in the art at the time of the invention was made to modify the probe card of Hirano et al with the receptacle probe card of Nakajima et al for the purpose of replacing different probe card to match with different device under test.

5. Claims 19 – 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirano et al (US 5,625,298) in view of Yanof et al (US 5,513,430).

As to claims 19, 20, Hirano et al disclose (fig 2) disclose everything except for the method of forming the holes comprises the laser drilling and etching.

On the other hand, Yanof et al teach (fig 2) the method of forming the holes (14) comprises the laser (27) drilling and etching .

It would have been obvious to one having an ordinary skill in the art at the time of the invention was made to use the laser for the purpose of forming tapered probes in the off angle situation.

As to claim 21, Hirano et al disclose (fig 2) the method wherein forming the conductive vias (not label) comprises forming doped regions that extend through the semiconductor die.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jimmy Nguyen whose telephone number is 571 –272-1965. The examiner can normally be reached on M - F from 9 to 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ramize Nestor, can be reached on 571-272-2034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JN.
Feb 7, 2006

VINH NGUYEN
PRIMARY EXAMINER
A.U. 2829
02/17/06